DACO SEMICONDUCTOR

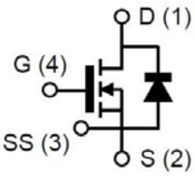
DAC015N065Z2

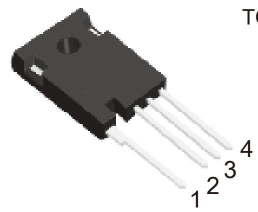
Silicon Carbide Enhancement Mode MOSFET

V_{DSS}	650V
$I_{D(@25°C)}$	120A
$R_{DS(ON)}$	15mΩ

Features

- Optimized package with separate driver source pin
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Qrr)





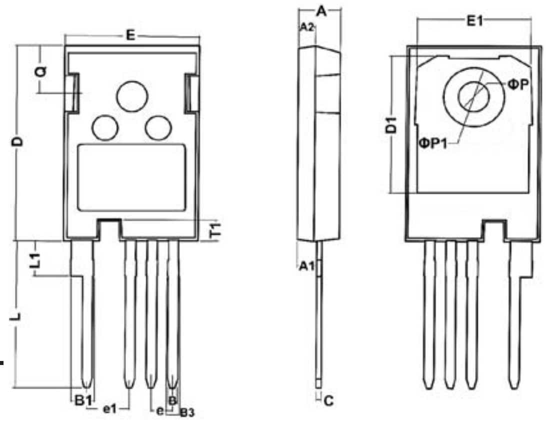
Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

Applications

- Solar inverters
- EV motor drive
- DC/DC converters
- UPS
- SMPS

Package Dimensions



Absolute Maximum Ratings

(Tc = 25℃ unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage	**V_{GS}=0V I_D=100μA**	**V_{DS}**	**650**	**V**
Gate-Source Voltage		**V_{GS}**	**-8/+19**	**V**
Drain Current-Continuous	**@ T_C =25°C @ T_C =100°C**	**I_D**	**120 95**	**A**
Pulse Drain Current		**$I_{D,pulse}$**	**400**	**A**
Power Dissipation	**@ T_C =25°C @ T_J =175°C**	**P_D**	**440**	**W**
Storage Temperature Range		**T_{STG}**	**-40 to +175**	**°C**
Operating Junction Temperature Range		**T_J**	**-40 to +175**	**°C**

Symbol	Dimensions in millimeters	
	Min.	**Min.**
A	4.80	5.20
A1	2.21	2.61
A2	1.80	2.20
B	1.06	1.36
B1	2.33	2.93
B3	1.07	1.60
C	0.51	0.75
D	23.30	23.60
D1	16.25	16.85
E	15.74	16.14
E1	13.72	14.32
T1	2.35	2.65
e	2.54 BSC	
e1	5.08 BSC	
Q	5.49	6.09
L	17.27	17.87
L1	3.99	4.39
ØP	3.40	3.80
ØP1	7.19 REF	

Electrical Characteristics @ T_C =25°C (unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
OFF Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V , I_{DS}=0.1mA	650	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V , V_{DS}=650V	-	1	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=15V , V_{DS}=0V	-	10	250	nA
ON Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS} , I_{DS}=16mA	1.8	2.3	3.6	V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS}=15V , I_{DS}=60A	11	15	20	mΩ
Transconductance	g_{fs}	V_{DS}=20V , I_{DS}=60A	-	43	-	S
Dynamic Characteristics						
Input Capacitance	C_{iss}	V_{DS}=400V V_{GS}=0V V_{AC}=25mV Freq.=100KHz	-	5000	-	pF
Output Capacitance	C_{oss}		-	290	-	pF
Reverse Transfer Capacitance	C_{rss}		-	32	-	pF
C_{OSS} Stored Energy	E_{oss}		-	28	-	μJ
Turn-On Switching Energy	E_{on}	V_{DD}=400V , V_{GS}=-4V/+15V I_D =60A , $R_{G(ext)}$ =5.0Ω L=57.6μH , T_J =175°C	-	400	-	μJ
Turn-Off Switching Energy	E_{off}		-	250	-	μJ
Switching Characteristics						
Turn-On Delay Time	$t_{d(on)}$	V_{DS}=400V V_{GS}=-4/+15V I_D=60A , L=57.6μH $R_{G(ext)}$ =5.0Ω Timing relative to V_{DS}, Inductive load	-	22	-	ns
Rise Time	t_r		-	31	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	58	-	ns
Fall Time	t_f		-	13	-	ns
Total Gate Charge	Q_g	V_{DS}=400V V_{GS}=-4/+15V I_D =60A	-	190	-	nC
Gate to Source Charge	Q_{gs}		-	54	-	nC
Gate to Drain Charge	Q_{gd}		-	59	-	nC
Body Diode Characteristics						
Inverse Diode Forward Voltage	V_{SD}	V_{GS}=-4V , I_{SD}=28A T_J =25°C	-	4.8	-	V
Continuous Diode Forward Current	I_S	V_{GS}=-4V , T_C=25°C	-	-	80	A
Reverse Recovery Time	T_{rr}	V_{GS}=-4V I_{SD}=60A , V_{DS}=400V, di/dt=4000A/μs T_J=175°C	-	25	-	ns
Reverse Recovery Charge	Q_{rr}		-	550	-	nC
Peak Reverse Recovery Current	I_{rrm}		-	38	-	A
Thermal Resistance						
Thermal Resistance, Junction-to-Case	$R\theta_{JC}$		-	0.34	-	°C/W

Typical Device Performance

Fig 1. Output characteristics, T_J = -40 °C (1st quadrant , t_p = < 200 μs)

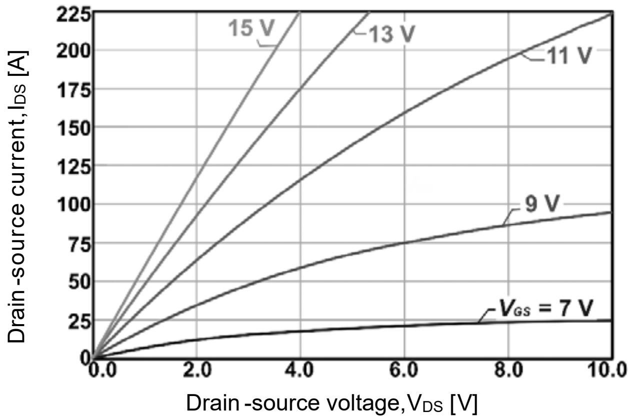


Fig 2. 3rd Qutput characteristics, T_J = -40 °C (t_p = < 200 μs)

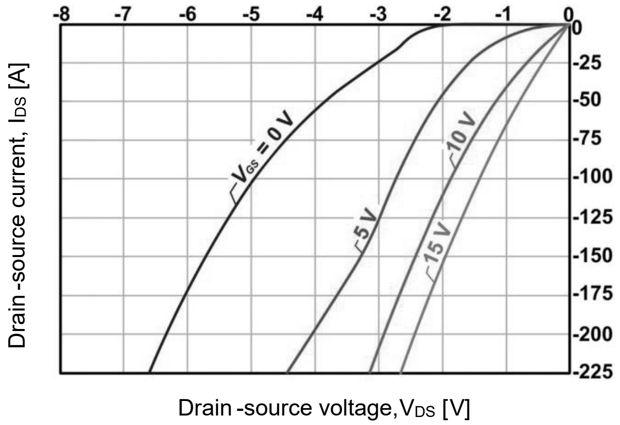


Fig 3. Output characteristics, T_J = 25 °C (1st quadrant , t_p = < 200 μs)

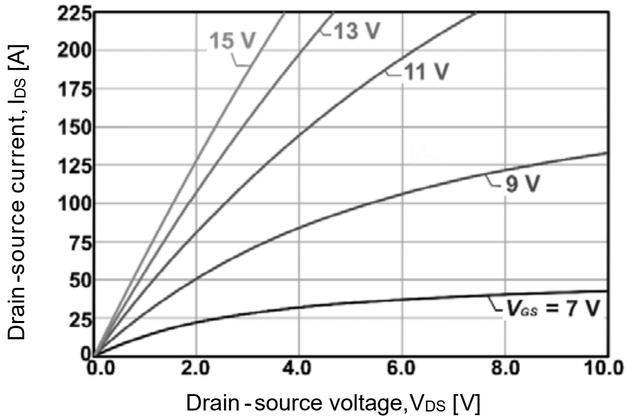


Fig 4. 3rd Qutput characteristics, T_J = 25 °C (t_p = < 200 μs)

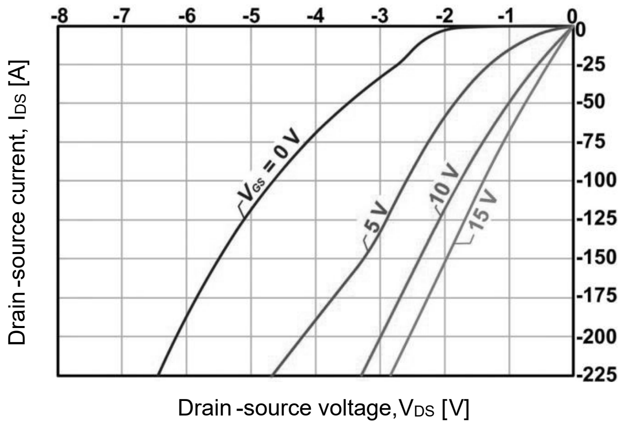


Fig 5. Output characteristics, T_J = 175 °C (1st quadrant , t_p = < 200 μs)

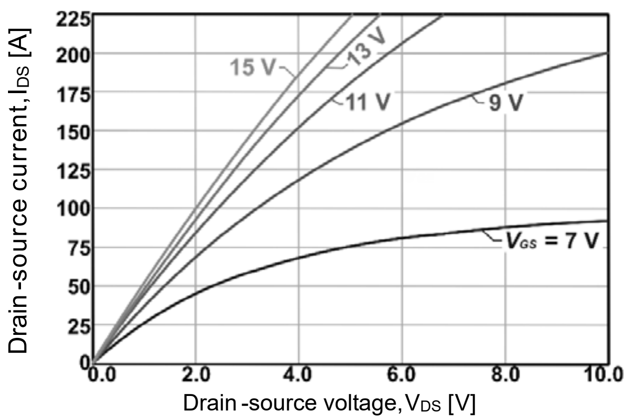


Fig 6. 3rd Qutput characteristics, T_J = 175°C (t_p = < 200 μs)

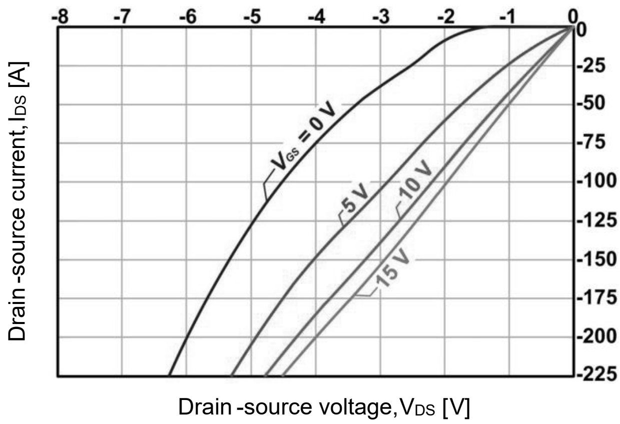


Fig 7. Transfer characteristic for various junction temperatures (V_{DS} = 20 V, t_p < 200 µs)

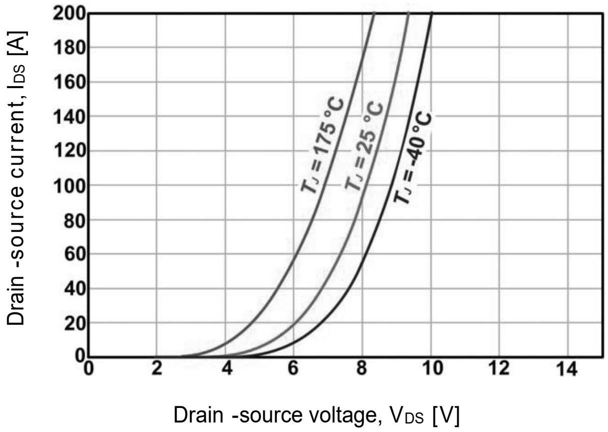


Fig 8. Normalized on-resistance vs. Temperatures (I_{DS} = 60 A, V_{GS} = 15 V, t_p < 200 µs)

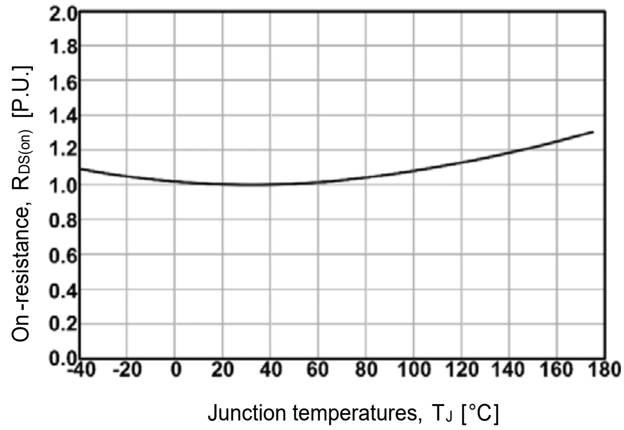


Fig 9. On-resistance vs. Drain current (V_{DS} = 15 V, t_p < 200 µs)

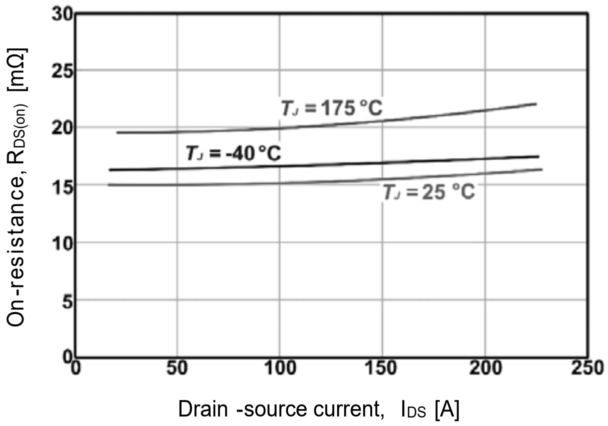


Fig 10. On-resistance vs. temperature for various gate voltage (I_{DS} = 60 A, V_{GS} = 15 V, t_p < 200 µs)

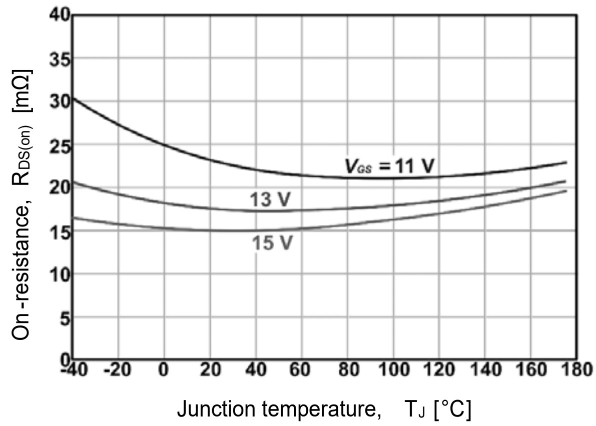


Fig 11. Body diode characteristic, T_J = -40 °C (t_p < 200 µs)

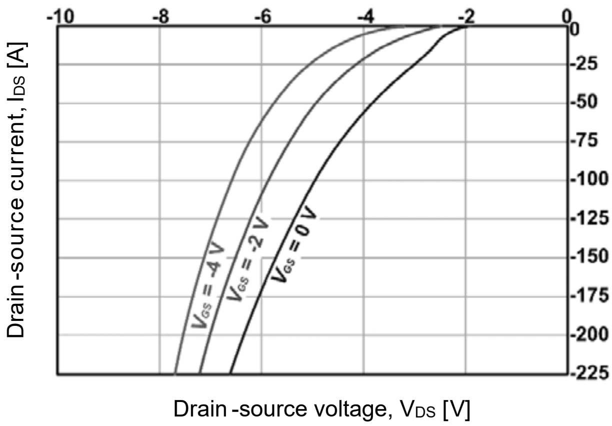


Fig 12. Body diode characteristic, T_J = 25 °C (t_p < 200 µs)

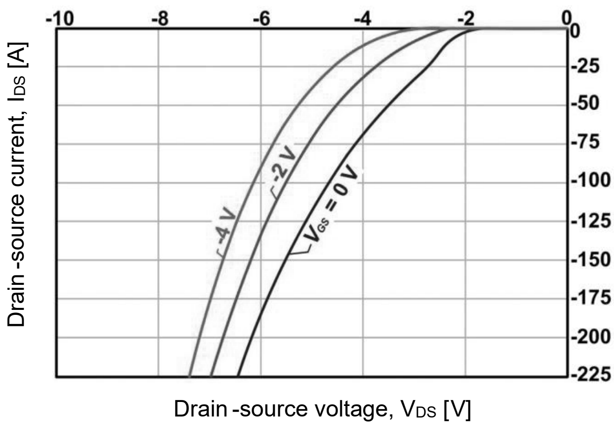


Fig 13. Body diode characteristic, T_J = 175 °C (t_p < 200 μs)

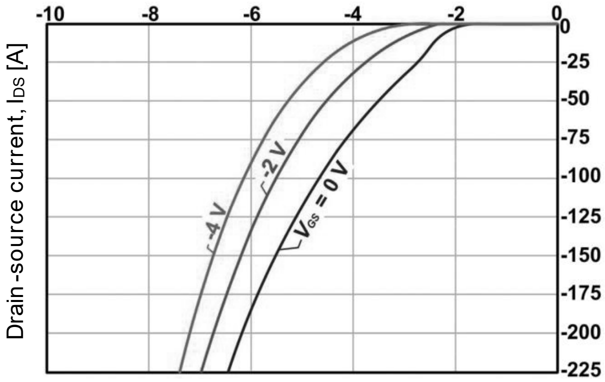


Fig 14. Threshold voltage vs. Temperature (V_{GS} = V_{DS}, I_D = 16 mA)

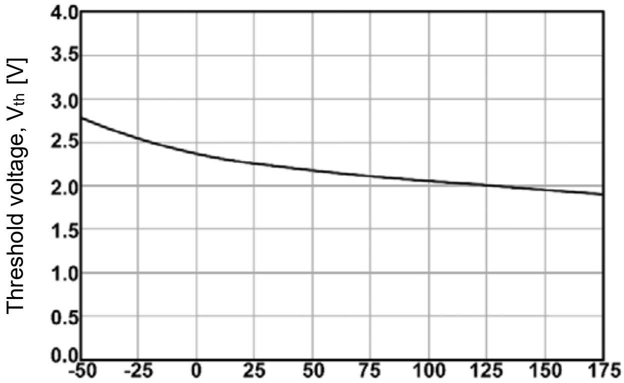


Fig 15. Capacitance vs. Drain-source voltage (0-200 V) (T_j = 25 °C, V_{AC} = 25 mV, f = 1 MHz)

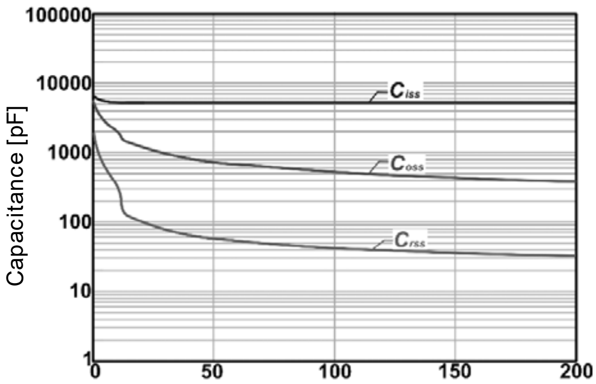


Fig 16. Capacitance vs. Drain-source voltage (0-650V) (T_j = 25 °C, V_{AC} = 25 mV, f = 1 MHz)

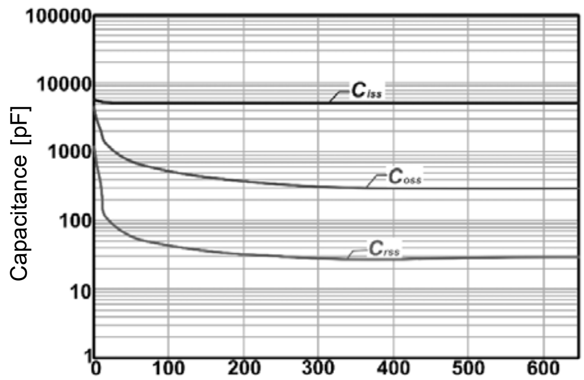


Fig 17. Output capacitance stored energy

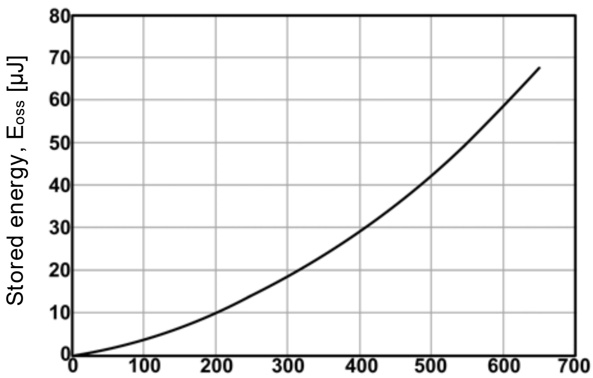


Fig 18. Gate charge characteristics (I_{DS} = 60 A, I_{GS} = 50 mA, V_{DS} = 400 V, T_j = 25 °C)

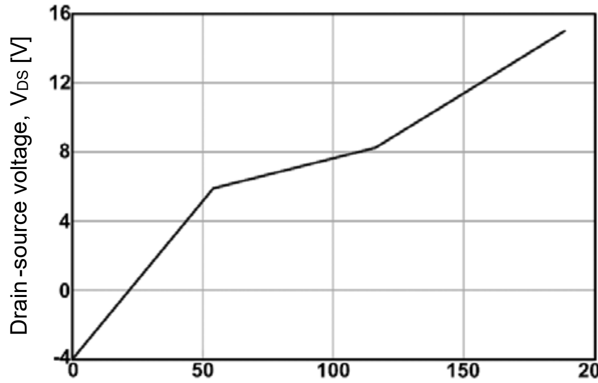


Fig 19. Continuous drain current derating vs. Case Temperature, T_J = 175 °C

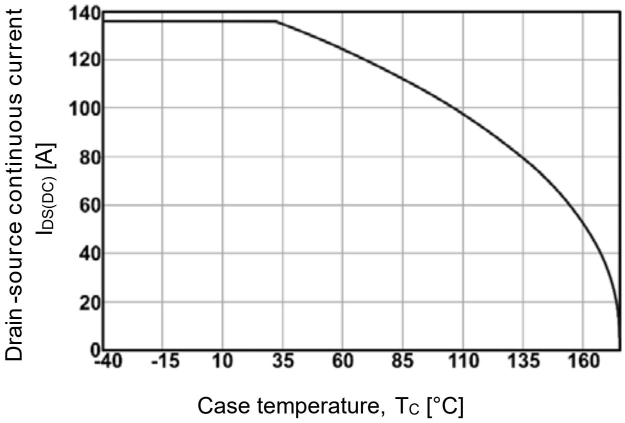


Fig 20. Maximum power dissipation derating vs. Case temperature, T_J = 175 °C

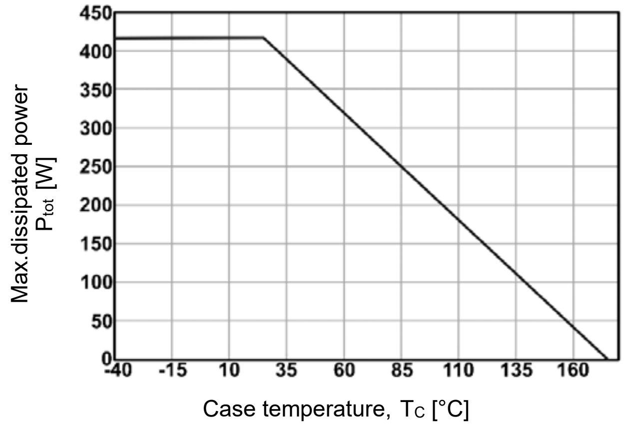


Fig 21. Safe operating area

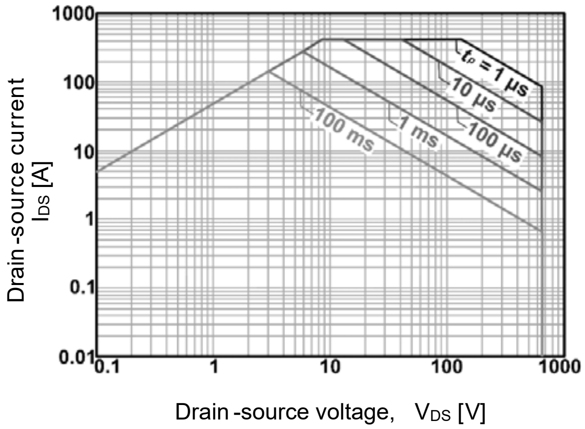


Fig 22. Transient thermal impedance (Junction - Case)

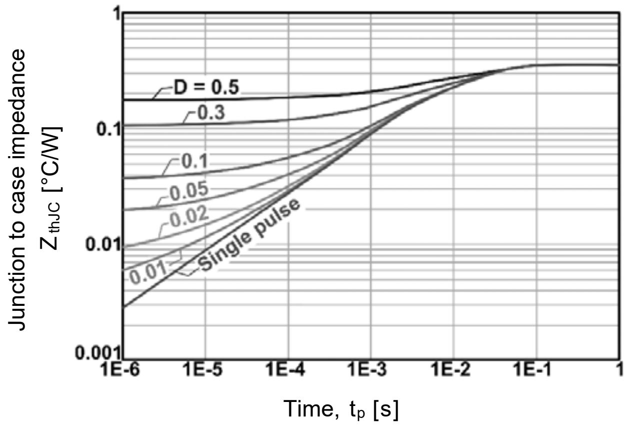


Fig 23. Clamped inductive switching energy vs. Drain current (V_{DD} = 400 V, T_j = 25 °C, V_{GS} = -4 / +15 V, L = 57.6 µH, $R_{G(ext)}$ = 5 Ω, FWD = SiC SBD)

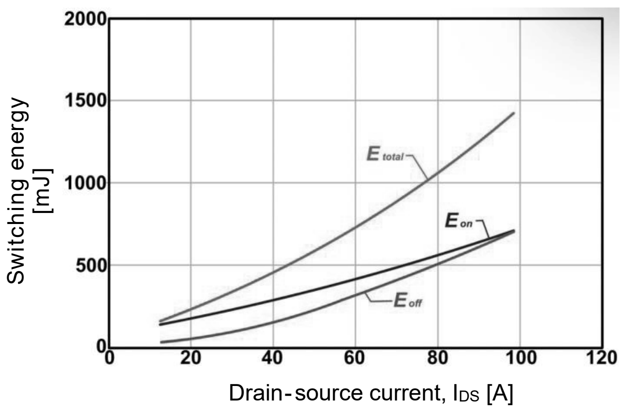


Fig 24. Clamped inductive switching energy vs. Drain current (T_j = 25 °C, V_{DD} = 400 V, I_{DS} = 60 A, V_{GS} = -4 / +15 V, L = 57.6 µH, FWD = SiC SBD)

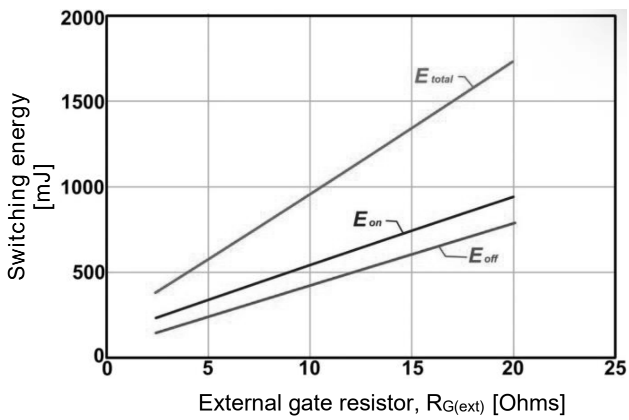


Fig 25. Clamped inductive switching energy vs. Temperature
(I_{DS} = 60 A, V_{DD} = 400 V, $R_{G(ext)}$ = 5 Ω, V_{GS} = -4 / +15 V, L = 57.6 μH, FWD =SiC SBD)

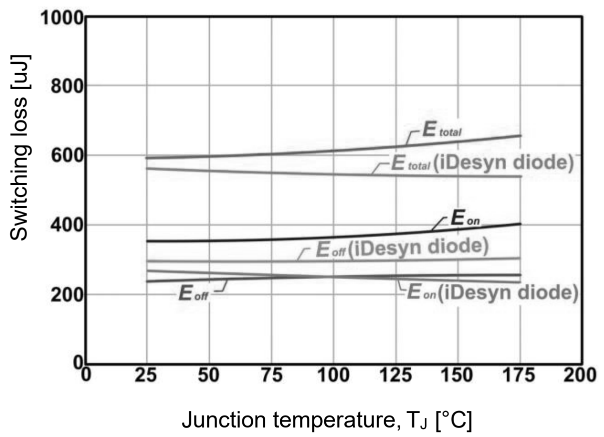


Fig 26. Switching times vs. $R_{G(ext)}$
(T_j = 25 °C, V_{DD} = 400 V, I_{DS} = 60 A, V_{GS} = -4 / +15 V, FWD = SiC SBD)

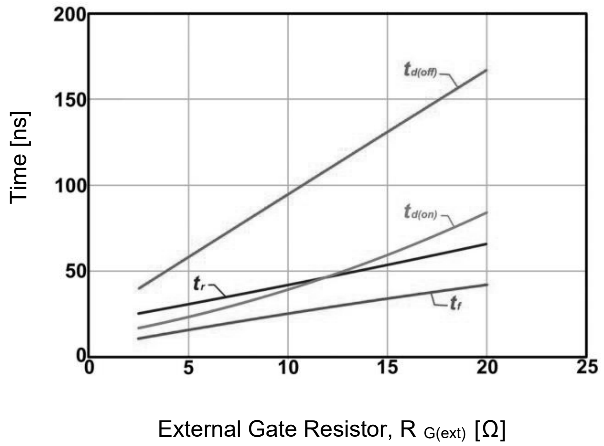


Fig 27. Clamped inductive switching waveform test circuit

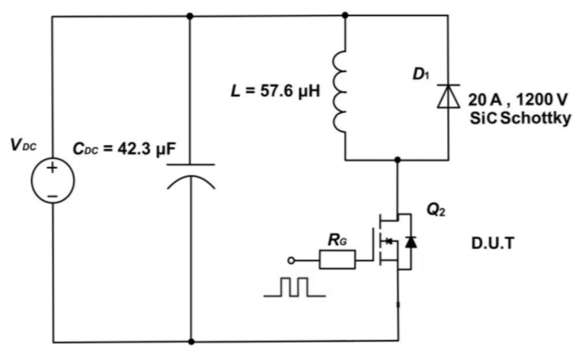
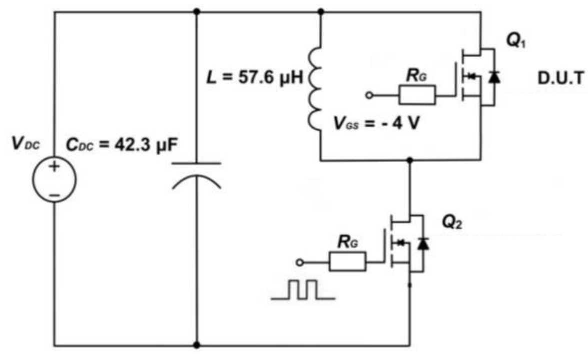


Fig 28. Body diode recovery test circuit



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